M.S.P. Mandal's
Shri Shivaji Institute of Engineering & Management Studies,
Vasmat Road, Parbhani – 431 401 (M.S.).
Ph. (02452) 234109, Fax (02452) 221958
Email: director.ssiems@gmail.com web: www.ssiems.org.in

DTE Code: 2252 **University Code: 2252**

Shri. Prakash Solanke	Shri. Satish Chavan	Shri. Anil Nakhate	Dr. Anand K. Pathrikar
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DVV Clarifications

3.3.2 Number of books and chapters in edited volumes/books published and papers published in national/ international conference proceedings per teacher during last five years

3.3.2.1. Total number of books and chapters in edited volumes/books published and papers in national/ international conference proceedings year wise during last five years

DVV Clarifications	HEI Response
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Cover Page

Advances in Intelligent Systems and Computing

Volume 1025

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Brijesh Iyer
Department of Electronics and
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Dr. Babasaheb Ambedkar
Technological University
Lonere, Maharashtra, India

S. C. Sharma
Department of Electronics
and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, Uttarakhand, India

P. S. Deshpande
Department of Computer Engineering
Dr. Babasaheb Ambedkar
Technological University
Lonere, Maharashtra, India

Ulhas Shiurkar
Deogiri Institute of Engineering
and Management Studies
Aurangabad, Maharashtra, India

ISSN 2194-5357 ISSN 2194-5365 (electronic)
Advances in Intelligent Systems and Computing
ISBN 978-981-32-9514-8 ISBN 978-981-32-9515-5 (eBook)
https://doi.org/10.1007/978-981-32-9515-5

This Springer imprint is published by the registered company Springer Nature Singapore Pte Ltd.
The registered company address is: 152 Beach Road, #21-01/04 Gateway East, Singapore 189721, Singapore

Editors
Brijesh Iyer
Department of Electronics and
Telecommunication Engineering
Dr. Babasaheb Ambedkar
Technological University
Lonere, Maharashtra, India

S. C. Sharma
Department of Electronics
and Computer Engineering
Indian Institute of Technology Roorkee
Roorkee, Uttarakhand, India

P. S. Deshpande
Department of Computer Engineering
Dr. Babasaheb Ambedkar
Technological University
Lonere, Maharashtra, India

Ulhas Shiurkar
Deogiri Institute of Engineering
and Management Studies
Aurangabad, Maharashtra, India

ISSN 2194-5357 ISSN 2194-5365 (electronic)
Advances in Intelligent Systems and Computing
ISBN 978-981-32-9514-8 ISBN 978-981-32-9515-5 (eBook)
https://doi.org/10.1007/978-981-32-9515-5

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Design of Power-Efficient 5- to 32-Row Decoder for 1 KB SRAM Using VLSI Technology

Conference paper | First Online: 17 October 2019

pp 625–636 | Cite this conference paper

A. K. Pathrikar ✉ & Rajkumar S. Deshpande

Part of the book series: Advances in Intelligent Systems and Computing ((AISC,volume 1025))

Abstract

In this paper we have designed power-efficient 5–32-row decoder, which is further going to be used as a component in 1 KB SRAM. The schematics of all the components of 5–32-row decoder are primarily designed and simulated using advanced design system (ADS) and the layouts of all components are then implemented and analyzed at chip level using Microwind 3.1-a layout editor. The 45 and 32 nm technologies are used to design and analyze scaling effect and performance of row decoder. Our focus will be to reduce the size, improve the power consumption and also to improve the response time of row decoder. The analysis proves that the performance parameters, that is, size, power consumption, access time, speed and frequency, of the 5–32-row decoder are improved approximately 30%. Hence the technology scaling, that is, 45 and 32 nm increases the overall performance by 30%.

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