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Cover Page

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Volume 1025

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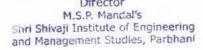
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First Page of Referenced Publications

Design of Power-Efficient 5- to 32-Row Decoder for 1 KB SRAM Using VLSI Technology

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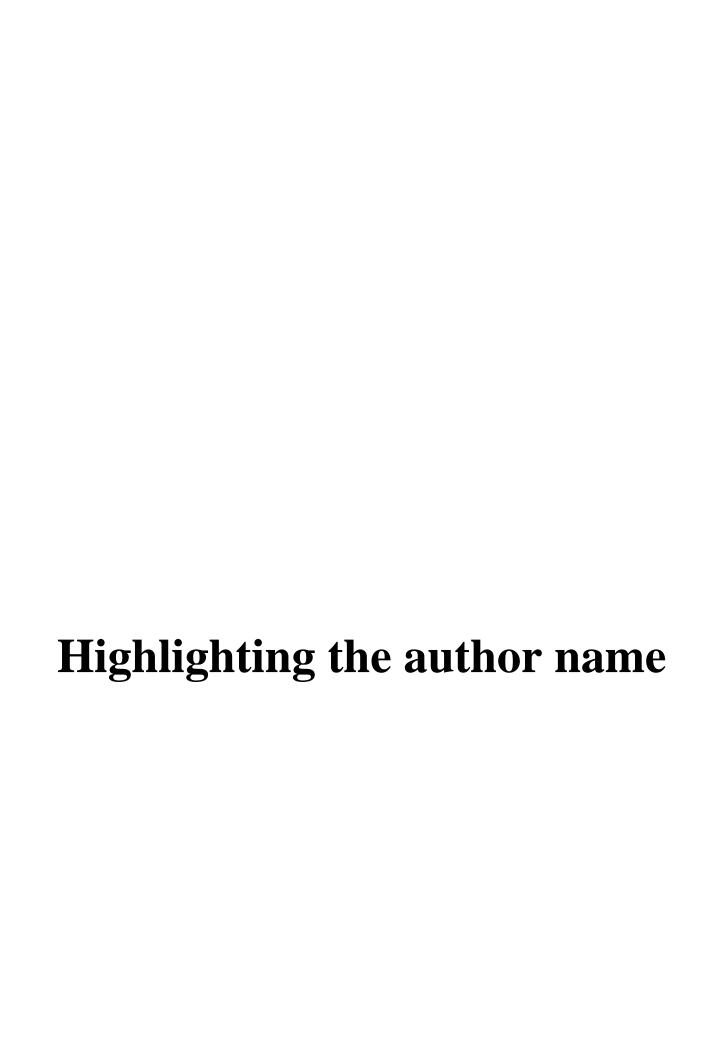
A. K. Pathrikar A & Rajkumar S. Deshpande

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Abstract

In this paper we have designed power-efficient 5–32-row decoder, which is further going to be used as a component in 1 KB SRAM. The schematics of all the components of 5–32-row decoder are primarily designed and simulated using advanced design system (ADS) and the layouts of all components are then implemented and analyzed at chip level using Microwind 3.1-a layout editor. The 45 and 32 nm technologies are used to design and analyze scaling effect and performance of row decoder. Our focus will be to reduce the size, improve the power consumption and also to improve the response time of row decoder. The analysis proves that the performance parameters, that is, size, power consumption, access time, speed and frequency, of the 5–32-row decoder are improved approximately 30%. Hence the technology scaling, that is, 45 and 32 nm increases the overall performance by 30%.



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